Designing FET's for Broad Noise Circles

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Abstract— **This paper shows that the keys to broader noise circles are a lower minimum noise figure and a small optimum generator reflection coefficient. There is an optimum FET width for the smallest generator reflection coefficient and the broadest noise circles. This was demonstrated with 0.25 μm MODFET's. A FET of optimum width also has the lowest noise figure with a 50 Ω generator. An expression is derived showing that the optimum gate width is inversely proportional to frequency, and that the optimum width should be a weak function of gate length for FET's optimally scaled for gate length.**

I. Introduction

BROAD noise circles for a FET are useful for manufacturing low-noise amplifiers that are used in a 50 Ω system. A manufacturer wants the noise figure of his amplifier to be equal to the minimum noise figure of the FET, $F_{\min}$. This is only obtained when the generator reflection coefficient is tuned to $\Gamma_{\rm opt}$. At any other generator impedance Γ_G, the noise figure F is higher. When a FET has broad noise circles, tuning to $\Gamma_{\rm opt}$ precisely is not critical for achieving a noise figure close to $F_{\min}$. Therefore, the low-noise amplifier is easier to manufacture. This paper shows that the key factors for designing FET's with broader noise circles are low $F_{\min}$ and a small $|\Gamma_{\rm opt}|$. $|\Gamma_{\rm opt}|$ is a function of gate width. It will be shown that there is an optimum FET width for the smallest $\Gamma_{\rm opt}$ and the broadest noise circles. Another reason that broad noise circles are sought is to obtain a good compromise between low-noise figure and high gain. This paper suggests that this compromise cannot be improved for intrinsic FET's.

The noise parameters and noise circles are modeled in this paper with an intrinsic FET model. Circuit concepts for the intrinsic FET are understandable and generally applicable to full circuit models of extrinsic FET's. FET noise parameters are modeled here with Pospieszalski's resistor temperature model [1], [2]. Expressions for the optimum generator impedance and other noise parameters are written directly for this noise model. The dependence of the modeled noise parameters on gate width and frequency was experimentally verified. This paper gives physical reasons why a low-noise FET that is matched for maximum gain has a noise figure close to 3 dB, and shows how this observation can be used to understand the width of FET noise circles. Finally, the paper gives an expression for the optimum gate width of FET's for broad noise circles which shows that the optimum width is inversely proportional to frequency.

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II. Noise Circles

The noise figure of an amplifier can be expressed as an equivalent input noise temperature of an amplifier T_e

$$F = 1 + \frac{T_e}{T_o} \tag{1}$$

where T_o is the standard temperature of the generator: 290 K. The dependence of T_e on generator impedance Z_G (or generator reflection coefficient Γ_G) can be modeled with four noise parameters: the minimum noise temperature $T_{\min}$, the optimum generator impedance ($Z_{\rm opt} = R_{\rm opt} + jX_{\rm opt}$), and a normalized parameter $\boldsymbol{n}$. The optimum generator reflection coefficient $\Gamma_{\rm opt}$, or optimum generator admittance ($Y_{\rm opt} = G_{\rm opt} + jB_{\rm opt}$), can be used instead of $Z_{\rm opt}$. Equation (2) gives the familiar constant noise figure circles on a Smith chart.

$$\begin{aligned} T_e &= T_{\min}\left[1 + \boldsymbol{n}\frac{|\Gamma_G - \Gamma_{\rm opt}|^2}{(1-|\Gamma_G|^2)(1-|\Gamma_{\rm opt}|^2)}\right] \\ &= T_{\min}\left[1 + \boldsymbol{n}\frac{(R_{\rm opt}-R_G)^2 + (X_{\rm opt}-X_G)^2}{4R_G R_{\rm opt}}\right]. \end{aligned} \tag{2}$$

When written in this form, the expression for noise temperature as function of generator impedance Z_G is very similar to the expression for available gain G_A [3].

$$\begin{aligned} \frac{1}{G_A} &= \frac{1}{G_{A\max}}\left[1 + \frac{|\Gamma_G - \Gamma_{\rm opt}^G|^2}{(1-|\Gamma_G|^2)(1-|\Gamma_{\rm opt}^G|^2)}\right] \\ &= \frac{1}{G_{A\max}}\left[1 + \frac{(R_{\rm opt}^G - R_G)^2 + (X_{\rm opt}^G - X_G)^2}{4R_G R_{\rm opt}^G}\right] \end{aligned} \tag{3}$$

where $G_{A\max}$ is the maximum available gain, which is equal to $(f_{\max}/f)^2$, and $Z_{\rm opt}^G$ is the generator impedance for maximum available gain. This expression is only applicable for FET's that are unconditionally stable.

The normalized noise parameter $\boldsymbol{n}$ is written in terms of conventional noise parameters in (4). $\boldsymbol{n}$ is independent of gate width (for the intrinsic FET) and it has a limited range of values close to 2 for low-noise FET's. $\boldsymbol{n}$ replaces N, R_n, and G_n in the usual reflection coefficient [3]–[6], impedance [1], [7], and conductance [4], [8] forms of the noise equation.

$$\boldsymbol{n} = \frac{4NT_o}{T_{\min}} = \frac{4T_o}{T_{\min}}\frac{R_{\rm opt}R_n}{|Z_{\rm opt}|^2} \tag{4}$$

$$N = R_n G_{\rm opt} = \frac{R_n R_{\rm opt}}{|Z_{\rm opt}|^2}. \tag{5}$$

$\boldsymbol{n}$ is discussed in more detail later, after the resistor temperature model has been reviewed in Section III. The expression for

noise figure is

$$F = F_{\min} + \frac{(F_{\min}-1)\boldsymbol{n}}{(1-|\Gamma_{\text{opt}}|^2)} \cdot \frac{|\Gamma_G - \Gamma_{\text{opt}}|^2}{(1-|\Gamma_G|^2)}$$
$$= F_{\min} + \frac{R_n |Z_{\text{opt}} - Z_G|^2}{R_G |Z_{\text{opt}}|^2}. \quad (6)$$

The second term of (6) describes how quickly F increases as Γ_G deviates from Γ_{opt}. If the second term increases slowly with $|\Gamma_G - \Gamma_{\text{opt}}|$, then the FET has broad noise circles. The noise circle term is proportional to $\boldsymbol{n}(F_{\min}-1)/(1-|\Gamma_{\text{opt}}|^2)$. Noise circles are broader for FET's with a lower $F_{\min}$ and a small $|\Gamma_{\text{opt}}|$. Γ_{opt} and $F_{\min}$ are not independent. Later, a model is used to show their relationship. There is an optimum gate width for minimum $|\Gamma_{\text{opt}}|$ and broadest noise circles because $|\Gamma_{\text{opt}}|$ is a much stronger function of gate width than $F_{\min}$ if the FET is made wider by adding fingers in parallel. This is discussed in Section IV.

The noise figure with a generator of 50 Ω, $F(50\,\Omega)$, is smallest for a FET designed with the optimum gate width for broadest noise circles. The reason is $|\Gamma_G - \Gamma_{\text{opt}}|$ becomes $|\Gamma_{\text{opt}}|$ and $|\Gamma_{\text{opt}}|$ is a minimum for broadest noise circles. $|\Gamma_{\text{opt}}|$ is smaller if X_{opt} is smaller. Namely, a FET with a larger input capacitance, but the same $F_{\min}$ and input resistance, has broader noise circles. However, redesigning FET's for larger input capacitance usually reduces gain and increases $F_{\min}$. FET design is discussed in more detail in Section VII. The broader noise circles for a FET with a smaller $|\Gamma_{\text{opt}}|$ is just a consequence of displaying the dependence of F on Z_G on a Smith chart.

The matching network between the generator and the FET input is not lossless, especially for MMIC's, because inductors and high impedance transmission lines are lossy. Therefore, the matching network increases the amplifier noise figure. For example, the noise figure of a 12 GHz DBS MMIC amplifier was 1.18 dB because of losses and noise from the second stage, despite the MODFET having an $F_{\min}$ of 0.48 dB [19]. In general, the losses of the matching network are proportional to the impedance transformation and the losses are less when $|\Gamma_{\text{opt}}|$ is smaller. A FET with a smaller $|\Gamma_{\text{opt}}|$ will not only have broader noise circles, but the final amplifier may also have a lower noise figure.

The $T_e/T_{\min}$ ratio is independent of $T_{\min}$ for a given Γ_G and Γ_{opt} [see (2)]. Namely, the percentage increase in noise temperature, as Γ_G deviates from Γ_{opt}, is a weak function of $T_{\min}$ because it only depends on $\boldsymbol{n}$. A noise circle at a fixed $T_e/T_{\min}$ ratio is usually more useful than a noise circle 1 dB higher than $F_{\min}$. F being 1 dB higher than $F_{\min}$ is much more significant for a FET with an $F_{\min}$ of 0.6 dB than for a FET with an $F_{\min}$ of 3 dB.

III. Resistor Temperature Model

The dependence of noise parameters and noise circles on $F_{\min}$, gate width, and frequency are modeled with an intrinsic FET model. An equivalent circuit of the intrinsic FET is shown in Fig. 1. Noise is modeled as thermal noise from the input resistor r_{gs}, and the output resistor R_{ds} [1]. These resistors have noise temperatures T_g and T_d, respectively. Pospieszalski showed that T_g is close to ambient and the temperatures are uncorrelated for intrinsic FET's [1]. Pospieszalski's model is not only simple and physically appealing, but it also accurately models experimentally measured noise parameters.

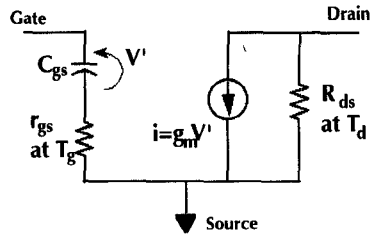

Fig. 1. Equivalent circuit of the intrinsic FET for the noise model.

The simple intrinsic FET equivalent circuit model topology can be used to simulate measured S-parameters of extrinsic FET's at frequencies much less than $f_{\max}$ [32]. Parameter values for the simple intrinsic model topology are extracted directly from measured Y- parameters [33], [34]. Small parasitics only change parameter values of the intrinsic FET model topology, but do not change the frequency dependence of the Y-parameters at frequencies much less than $f_{\max}$. Similarly, an effective T_d can be assigned to the effective R_{ds} to simulate measured noise parameters. For a typical extrinsic low-noise FET, the effective T_d is 500 K [2], which is much less than the extrinsic value because the extrinsic $f_{\max}$ is proportionally lower than the intrinsic $f_{\max}$. This simple intrinsic FET circuit and noise model is used in this paper to make the analysis and expressions understandable. The intrinsic FET model is applied to extrinsic FET's to demonstrate that the concept are applicable in practice. The intrinsic FET model is not intended for accurate modeling or circuit design at high frequencies.

The generator impedance for maximum available gain, Z^G_{opt}, is easy to predict for the simple, unilateral FET model shown in Fig. 1. The generator resistance for maximum gain R^G_{opt} is r_{gs}. The generator reactance for minimum noise figure is the same as that for maximum available gain for the intrinsic FET. X_{opt} is $j/(2\pi f C_{gs})$, where f is frequency.

The noise parameters $T_{\min}, R_{\text{opt}}$, and $\boldsymbol{n}$ are a function of only T_g and $T_d/G_{A\max}$ (or $T_d * (f/f_{\max})^2$)

$$T_{\min} = (T_g T_d)^{1/2} \frac{f}{f_{\max}} \left(\left(1 + \frac{T_d}{4T_g} \left(\frac{f}{f_{\max}} \right)^2 \right)^{1/2} + \left(\frac{T_d}{4T_g} \right)^{1/2} \frac{f}{f_{\max}} \right)$$
$$\approx (T_g T_d)^{1/2} \frac{f}{f_{\max}}. \quad (7)$$

The approximate expression predicts that $T_{\min}$ increases linearly with frequency like the Fukui approximation [7]. The approximation is only accurate for low $T_{\min}$. For example, when the full noise model predicts an $F_{\min}$ of 1.5 dB, the approximation predicts an $F_{\min}$ of 1.3 dB. R_{opt}/r_{gs} and $\boldsymbol{n}$ are expressed as either

TABLE I
NORMALIZED NOISE AND CIRCUIT MODEL PARAMETERS OF MODFET'S OF DIFFERENT GEOMETRIES. THE SIZE IS GIVEN AS THE NUMBER GATE FINGERS TIMES THE WIDTH OF EACH FINGER IN MICRONS

Size	$F_{\min}$	$G_{A\text{opt}}$	$R_{\text{opt}} \cdot W$	$R_{\text{in}} \cdot W$	$R_n \cdot W$	n	C_{opt}/W	C_{in}/W	f_T	$f_{\max}$	$Q_{\Gamma\text{opt}}$
# μm	dB	dB	$\Omega\cdot$ mm	$\Omega\cdot$ mm	$\Omega\cdot$ mm		pF/mm	pF/mm	GHz	GHz	
4 × 30	1.00	13.2	7.5	0.7	2.7	2.1	1.10	0.97	54	99	1.28
6 × 30	1.03	12.0	8.4	0.73	2.6	2.0	1.12	1.00	54	96	1.13
8 × 30	0.94	11.5	8.6	0.9	2.6	2.0	1.00	0.97	57	90	1.23
8 × 45	0.98	10.3	11.1	1.1	3.2	2.3	0.97	0.90	59	81	0.98
10 × 45	0.98	10.2	10.4	1.3	2.5	1.9	1.02	0.92	59	74	1.00

functions of T_g and $T_d * (f/f_{\max})^2$ or T_g and $T_{\min}$ [1], [2].

$$\frac{R_{\text{opt}}}{r_{gs}} = \frac{2T_g}{T_{\min}} + 1 \approx \left(\frac{4T_g}{T_d}\right)^{1/2} \frac{f_{\max}}{f} \tag{8}$$

$$\boldsymbol{n} = \frac{2 + \dfrac{T_{\min}}{T_g}}{1 + \dfrac{T_{\min}}{T_g}} \approx \frac{2}{1 + \left(\dfrac{T_d}{4T_g}\right)^{1/2} \dfrac{f}{f_{\max}}}. \tag{9}$$

The dependence of R_{opt}/r_{gs} on $F_{\min}$ in dB is shown in Fig. 2 for a fixed T_g of 298 K. This plot was generated by sweeping frequency for a given T_d. The plot shows that the R_{opt}/r_{gs} ratio is approximately inversely proportional $F_{\min}$ in dB [2]. Consequently, the difference between the reflection coefficient for maximum gain, Γ_{opt}^G, and minimum noise figure, Γ_{opt}, increases with decreasing $F_{\min}$. R_{opt}/r_{gs} is also a unique function of the ratio of frequency to $f_{\max}$, $(f/f_{\max})$, for a given T_g and T_d as shown in Fig. 3. Also shown in Fig. 3 is the $1/f$ approximation given by (8). The approximation is made for $2T_g/T_{\min}$ much larger than 1 and substituting the $T_{\min}$ approximation from (7). A comparison of the full model and the $1/f$ approximation shown in Fig. 3 demonstrates that the approximation is surprisingly accurate. The error is only 5% at an $f/f_{\max}$ of 0.5 (or $F_{\min}$ of 2.8 dB). The R_{opt}/r_{gs} and $T_{\min}$ approximations appear to compensate each other. R_{opt}/r_{gs} is inversely proportional to frequency to frequencies approaching $f_{\max}$.

Experimental data are shown in Figs. 2 and 3 to demonstrate the validity of the model. The data are for an extrinsic pseudomorphic MODFET with a gate width of 120 μm (4 × 30) and 0.25 μm gate length. The R_{opt} of the extrinsic FET showed the same dependence on $F_{\min}$ and frequency as predicted by the resistor temperature noise model for intrinsic FET's. The values of $f_{\max}$ and $r_{gs} \cdot W$ were chosen for agreement between measurement and model; the values were 100 GHz and 0.7 $\Omega\cdot$ mm, respectively. These values are consistent with the values extracted from Y-parameters and shown in Table I for MODFET's of different sizes from the same wafer.

$\boldsymbol{n}$ can only have values between 1 and 2 if the noise temperatures, T_g and T_d, are uncorrelated. $\boldsymbol{n}$ is close to 2 for low-noise FET's. $\boldsymbol{n}$ is between 1.8 and 2.0 for frequencies less than $0.1 \cdot f_{\max}$. Therefore, the noise circles are relatively

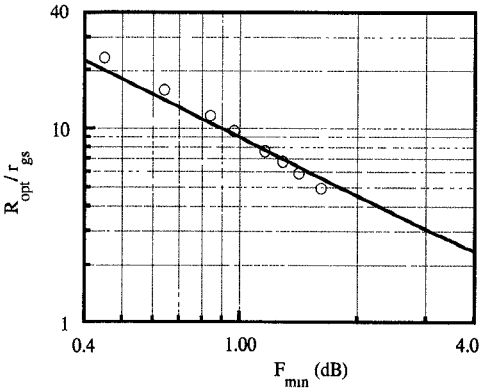

Fig. 2. Log-log plot of the ratios R_{opt}/r_{gs} versus $F_{\min}$ for a T_g of 298 K. ○ represents experimental data for 4 × 30 0.25 μm pseudomorphic MODFET. The data were plotted for an $r_{gs} \cdot W$ of 0.7$\Omega\cdot$ mm.

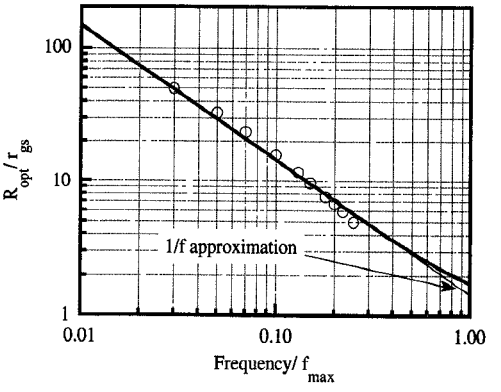

Fig. 3. Plot of the ratios R_{opt}/r_{gs} versus frequency normalized to $f_{\max}$ for a T_g of 298 K and a T_d of 550 K. ○ represents experimental data for a 4 × 30 0.25 μm pseudomorphic MODFET. The data were plotted for an $f_{\max}$ of 100 GHz and an $r_{gs} \cdot W$ of 0.7 $\Omega\cdot$ mm.

easy to estimate for an intrinsic FET if $T_{\min}$ and the circuit model (or Γ_{opt}) are known. For extrinsic FET's, with reactive feedback parasitics C_{gd} and L_s, $\boldsymbol{n}$ can be larger than 2. Typically, it is between 1.8 and 2.2 for low-noise extrinsic FET's. Experimental examples are shown in Table I. $\boldsymbol{n}$ can be plotted as a function of $F_{\min}$ for a given T_g, or as function of $f/f_{\max}$ for given T_g and T_d.

The associated gain when the FET is matched for $F_{\min}$, $G_{A\text{opt}}$, is much less than $G_{A\max}$ for low-noise FET's because the generator does not match the FET input. The $G_{A\text{opt}}/G_{A\max}$ ratio is a function of R_{opt}/r_{gs} only. Therefore,

$G_{A\text{opt}}/G_{A\max}$ is also a function of $T_{\min}$ and T_g only [2].

$$\frac{G_{A_{\text{opt}}}}{G_{A\max}} = \frac{2T_{\min}}{T_g}\frac{\left(1+\frac{T_{\min}}{2T_g}\right)}{\left(1+\frac{T_{\min}}{T_g}\right)^2} \approx \frac{2T_{\min}}{T_g} \tag{10}$$

$$G_{A_{\max}} = \left(\frac{f_{\max}}{f}\right)^2 = \frac{f_T^2 R_{ds}}{f^2 4 r_{gs}} \tag{11}$$

$$G_{A_{\text{opt}}} \approx G_{A\max} 4\frac{r_{gs}}{R_{\text{opt}}} \approx \left(\frac{4T_d}{T_g}\right)^{1/2}\frac{f_{\max}}{f}. \tag{12}$$

$G_{A_{\max}}$ is inversely proportional to frequency squared. It decreases at 6 dB per octave. For low-noise FET's ($F_{\min}$ less than 1.5 dB), $T_{\min}$ increases linearly with frequency [(7)]. Therefore, $G_{A_{opt}}$ decreases at 3 dB per octave.

The noise parameter most typically given on FET data sheets to rate the breadth of noise circles is R_n. R_n is written in terms of the resistor temperature noise model for comparison.

$$R_n = \frac{R_{\text{opt}}\boldsymbol{n}T_{\min}}{4T_o}\left[1+\frac{1}{(\omega C_{gs}R_{\text{opt}})^2}\right]$$
$$\approx r_{gs} + \left(\frac{T_d}{T_g R_{ds}}\right)\frac{1}{g_m^2}. \tag{13}$$

The expression shows that for low-noise FET's, R_n is a weak function of frequency. For a typical low-noise FET, the R_n/r_{gs} ratio is about 3.

IV. Scaling of FET Parameters with Gate Width

This section describes the dependence of $|\Gamma_{\text{opt}}|$ and the size of noise circles on gate width W for the intrinsic FET model. The circuit-model parameters scale simply with gate width for well-designed intrinsic FET's. C_{gs} and g_m are proportional to width. R_{ds} and r_{gs} are inversely proportional to width. Consequently, $G_{A_{\max}}$ is independent of width. $F_{\min}$ is independent of width because $G_{A_{\max}}, T_g$, and T_d are independent of width [(7)]. These scaling rules and (8)–(10) show that $\boldsymbol{n}, R_{\text{opt}}/r_{gs}$, and $G_{A_{\text{opt}}}$ are independent of width, and R_{opt} scales inversely with width. These simple scaling rules break down for very large FET's because of distributed effects, self-heating, and parasitic inductance, and they break down for very small FET's because of parasitic capacitances.

Although the simple intrinsic model cannot adequately describe the extrinsic FET's, the design principles should be applicable at frequencies much less than $f_{\max}$ (e.g., less than $0.2 \cdot f_{\max}$) where FET's are operated to obtain low $F_{\min}$ (e.g., $F_{\min}$ less than 1.2 dB). The parasitic resistances R_s, R_d, and r_{gd} scale like r_{gs}, and the feedback capacitance C_{gd} scales like C_{gs}. The gate resistance R_g scales like r_{gs} if the gate width is increased by adding fingers in parallel and the gate feed resistance is negligible. Experimental results presented in Section V (Table I) show that the extrinsic circuit model parameters and noise parameters scale reasonably well with gate width for extrinsic MODFET's.

The optimum generator reflection coefficients for maximum gain Γ_{opt}^G and minimum noise figure Γ_{opt} were calculated as a function of gate width of a MODFET. Plots of Γ_{opt} and Γ_{opt}^G as a function of gate width are shown in Figs. 4 and 5 for

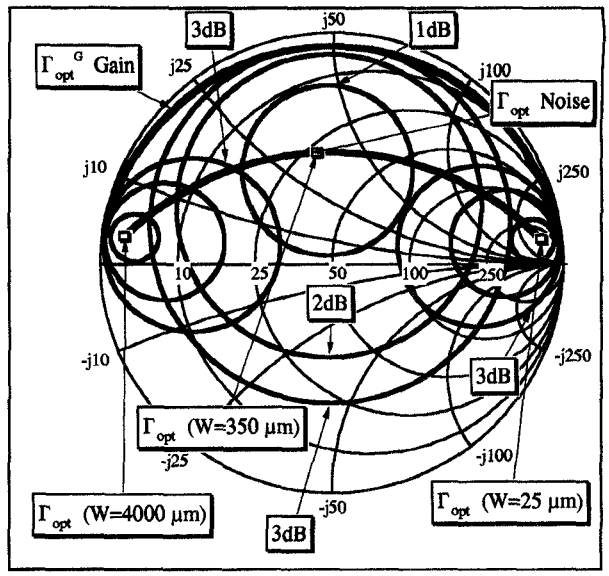

Fig. 4. Plots of Γ_{opt} and Γ_{opt}^G as a function of FET gate width W on a Smith chart. The model is for a FET at 12 GHz with an $F_{\min}$ of 0.69 dB, an $r_{gs} \cdot W$ of 0.8 ohm · mm, and a C_{gs}/W of 1.0 pF/mm. Plots are of the 1, 2, and 3 dB noise circles for FET's with widths of 25, 350, and 4000 μm.

frequencies of 12 and 36 GHz, respectively. The circuit model parameters were selected to simulate values of C_{gs}, f_T, and $f_{\max}$ for a typical extrinsic DBS MODFET. The MODFET, at low-noise bias, had an f_T of 50 GHz, an $f_{\max}$ of 100 GHz, a C_{gs}/W of 1.0 pF/mm, and an $r_{gs} \cdot W$ product of $0.8\,\Omega\cdot$ mm. The effective noise temperatures were 298 K for T_g and 500 K for T_d. The effective T_d of extrinsic FET's is much less than that of intrinsic FET's because the extrinsic $f_{\max}$ is much less than the intrinsic $f_{\max}$. These resistor temperatures give an $F_{\min}$ of 0.69 dB and a $G_{A_{\text{opt}}}$ of 12.7 dB at 12 GHz, which is typical for 0.25 μm conventional MODFET's [10]–[13].

Noise circles are shown for FET's of width 25, 350, and 4000 μm on Fig. 4. The noise circles are widest for the 350 μm wide FET. This FET has the smallest $|\Gamma_{\text{opt}}|$. The magnitude of Γ_{opt} is smallest when the angle of Γ_{opt} is 90°. The difference between Γ_{opt}^G and Γ_{opt} is a maximum at an angle of 90°. The 3 dB noise circles for each width almost touch the generator reflection coefficient contour for maximum gain Γ_{opt}^G. The noise figure of an amplifier matched for maximum gain must be at least 3 dB, and it is close to 3 dB for low-noise amplifiers. The reason for this is discussed in Section VI. When the FET width is optimum for broad noise circles, the FET has broad gain circles because $|\Gamma_{\text{opt}}^G|$ is also small.

Γ_{opt}^G and Γ_{opt} both follow constant Q contours on the Smith chart when plotted as functions of gate width, as shown in Figs. 4 and 5. The Q of $\Gamma_{\text{opt}}^G(W), Q_{\Gamma\text{opt}}^G$, is independent of width because $Q_{\Gamma\text{opt}}^G$ is $1/(2\pi f C_{gs} r_{gs})$ and C_{gs} is proportional to width, while r_{gs} is inversely proportional to width. $Q_{\Gamma\text{opt}}^G$ decreases with increasing frequency because the reactance is inversely proportional to frequency while the resistance is constant. The Q of $\Gamma_{\text{opt}}(W), Q_{\Gamma\text{opt}}$, is $1/(2\pi f C_{gs} R_{\text{opt}}) \cdot Q_{\Gamma\text{opt}}$, is a lower Q than $Q_{\Gamma\text{opt}}^G$, and it is also independent of width. $Q_{\Gamma\text{opt}}$ is almost independent of frequency because the $R_{\text{opt}} \cdot W$ product is inversely proportional to frequency while

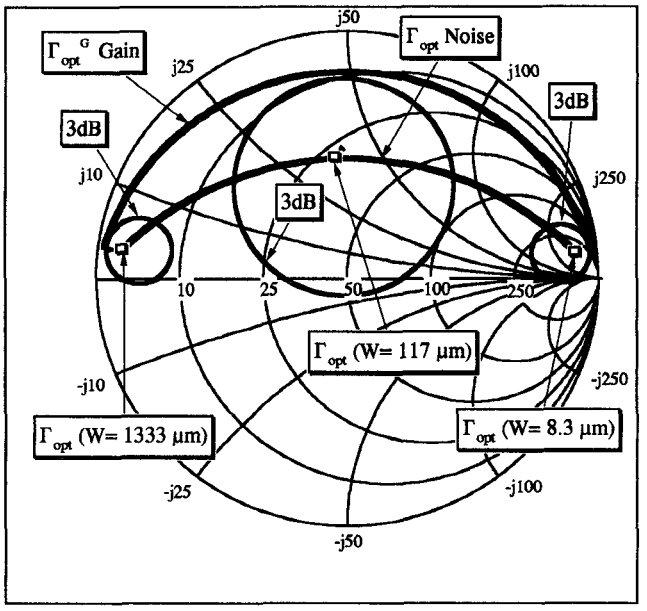

Fig. 5. Plots of $\Gamma_{\rm opt}$ and $\Gamma_{\rm opt}^{G}$ as a function of FET gate width on a Smith chart. The model is for a FET at 36 GHz with an $F_{\rm min}$ of 2.05 dB, an $r_{gs} \cdot W$ of 0.8 ohm · mm, and a C_{gs}/W of 1.0 pF/mm. Plots are of the 3 dB noise circles for FET's with widths of 8.3, 117, and 1333 μm.

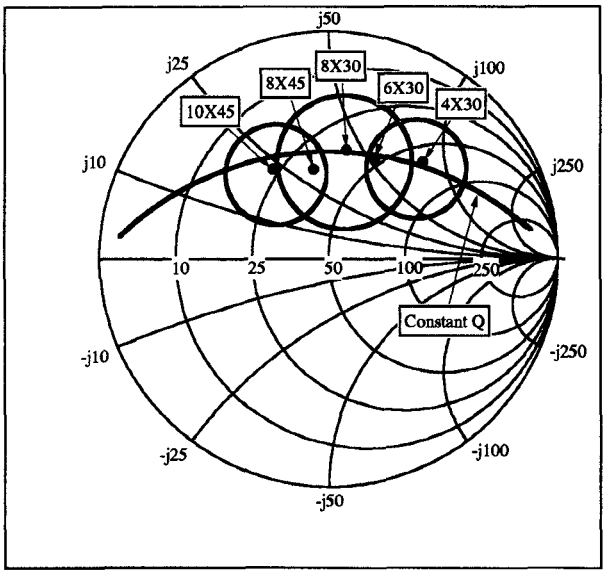

Fig. 6. Plots of the $\Gamma_{\rm opt}$'s for 0.25 μm pseudomorphic MODFET's of five different gate widths on a Smith chart. Plots are of a constant Q contour. Plots are of the 1.2 dB noise circles for the 4 × 30, 8 × 30, and 10 × 45 MODFET's.

the reactance is proportional to frequency. Comparing Figs. 4 and 5 shows that the Q's of the $\Gamma_{\rm opt}$ contours at 12 and 36 GHz are virtually identical. Only the range of widths is different for the two contours. The start width and the stop width at 36 GHz are 1/3 of the values at 12 GHz. The width for widest noise circles and smallest $|\Gamma_{\rm opt}|$ at 36 GHz is 117 μm, which is 1/3 of the optimum width at 12 GHz. The optimum width $W_{\rm opt}$ is inversely proportional to frequency. The $R_{\rm opt}$'s of FET's that are optimum width are independent of frequency because the $R_{\rm opt} \cdot W$ product and optimum gate width are inversely proportional to frequency. For a typical low-noise FET, $R_{\rm opt}(W_{\rm opt})$ is about 32 Ω.

V. Experimental Results

The noise parameters of 0.25 μm pseudomorphic MODFET's were measured for a range of gate widths. The MODFET design and fabrication methods are similar to those described previously [14]. The normalized noise parameters measured at 15 GHz are summarized in Table I. $C_{\rm opt}, C_{\rm in}$, and $R_{\rm in}$ in Table I are extracted from $1/(2\pi f X_{\rm opt}), 1/{\rm imag}(1/Y_{11})/(2\pi f)$ and real $(1/Y_{11})$, respectively. $C_{\rm in}$ and $R_{\rm in}$ are only used to distinguish parameters extracted from measurements and parameters of the intrinsic model parameters C_{gs} and r_{gs}. $C_{\rm in}$ and $C_{\rm opt}$ have similar values. $C_{\rm opt}$ is larger than $C_{\rm in}$ for extrinsic FET's because of the Miller effect. All the normalized parameters are a weak function of width. For example, $F_{\rm min}$ is 0.99 dB plus or minus 0.05 dB. n has values close to 2 for all widths. The standard deviation of dc (e.g., $g_m, I_{D\max}, R_s$, etc.) and circuit model element values (e.g., C_{gs}, g_m, etc.) are all less than 10% across the wafer. Most of the range of values in Table I can be attributed to typical variations across a wafer and noise figure measurement accuracy. However, a trend is discernible. The MODFET's with longer gate fingers had higher $R_{\rm in}$ and $R_{\rm opt}$ values and lower $G_{A\rm opt}$ and $f_{\rm max}$ values. This was expected for FET's with higher gate resistance. The $F_{\rm min}$ of the 8 × 45 MODFET's was higher than the $F_{\rm min}$ of the 8 × 30 MODFET, as expected. However, the $F_{\rm min}$ of the 4 × 30 and 6 × 30 were slightly (0.06–0.09 dB) higher than the 8 × 30 MODFET. Parasitic pad capacitance results in a higher $C_{\rm in}/W$ and $C_{\rm opt}/W$ and a lower f_T for the narrower gate width (4 × 30 and 6 × 30) MODFET's.

$\Gamma_{\rm opt}$ is plotted for different gate widths on a Smith chart in Fig. 6. The $\Gamma_{\rm opt}$'s of the MODFET's with 30 μm gate fingers lie close to the constant Q contour shown. The MODFET's with 45 μm gate fingers have a slightly lower Q because of their higher gate resistance, and their $\Gamma_{\rm opt}$'s are inside the contour. The $Q_{\Gamma\rm opt}$ of the experimental data is given in Table I. Also shown in Fig. 6 are the 1.2 dB noise circles for the 4 × 30, 8 × 30, and 8 × 45 MODFET's generated with the measured noise parameters for each MODFET. 1.2 dB circles were chosen so that the circles were small and easily distinguished. The noise circle of the 8 × 30 MODFET is clearly wider than those of the widest (10 × 45) and narrowest (4 × 30) MODFET's. The angle of $\Gamma_{\rm opt}$ for the 8 × 30 MODFET is 81°, which is close to the optimum of 90° predicted by the model. The prediction for noise circle width and optimum width are observed even with the limited range of gate widths presented here. The size of the noise circles do not change quickly with gate width, therefore, it is not necessary to find $W_{\rm opt}$ precisely. The noise parameters scale well for the extrinsic MODFET's, and the resistor temperature noise model predicts their behavior.

VI. Noise Figure of a Matched FET

An expression for the noise figure of a matched intrinsic FET is found by substituting the equations for the noise parameters [(8) and (9)] into the noise circle [(1) and (2)] for

the case of a generator impedance of $Z^G_{\rm opt}(r_{gs}+j/(2\pi fC_{gs}))$. It is assumed that T_g is equal to T_o (290 K) to simplify the algebra. The expressions for T_e and F are

$$T_e(Z^G_{\rm opt}) = T_g + \frac{T^2_{\rm min}}{T_g + T_{\rm min}} \tag{14}$$

$$F(Z^G_{\rm opt}) = 2 + \frac{(F_{\rm min}-1)^2}{F_{\rm min}}. \tag{15}$$

The expressions show that the noise figure of a FET matched for gain must be at least 3 dB and close to 3 dB for low-noise FET's because their $T_{\rm min}$ is much less than T_g. This is also evident in Figs. 4 and 5. The 3 dB noise circles appear to touch the $\Gamma^G_{\rm opt}$ contour in Fig. 4 where the FET has an $F_{\rm min}$ of 0.69 dB. For the FET's with $F_{\rm min}$ of 2.05 dB, shown in Fig. 5, the 3 dB noise circles are close to the $\Gamma^G_{\rm opt}$ contour, but do not touch.

The reason that the noise figure for a FET matched for gain is almost 3 dB is quite simple. Noise figure is defined as the ratio of noise powers available at the output of the amplifier [15]:

$$F = \frac{\text{total output noise power}}{\text{output noise power engendered from generator at 290 K}} \tag{16}$$

The thermal noise power at the output from the generator resistor and from the input resistor are almost equal because the input and generator resistances are the same and noise temperatures are almost equal (R_G equals r_{gs}, and T_g is approximately T_o). Consequently, the noise figure is at least 3 dB. The associated gain of the FET matched for gain is very high (i.e., $G_{A\,\rm max}$), therefore, the input noise is greatly amplified. The thermal noise from the output resistor (R_{ds} at T_d) is very small in comparison. Consider the example given in Fig. 4; $G_{A\,\rm max}$ is 18.4 dB at 12 GHz, so the equivalent output noise temperature from the input resistor at 298 K is 20 616 K. The output resistor at 500 K contributes only 2.4% of the output noise power. Therefore, the noise figure is not significantly greater than 3 dB for this matched low-noise FET.

The predicted F of a matched FET was not easily confirmed with comparisons to the published results because noise and gain circles have been shown only in a few recent publications [9], [16]. Other papers give S_{11} and noise circles [17], [18], so here it is assumed S^*_{11} indicates an approximate position of $\Gamma^G_{\rm opt}$. The results agree reasonably with this paper's model. $X_{\rm opt}$ and $X^G_{\rm opt}$ are similar. $R_{\rm opt}$ is always larger than $R^G_{\rm opt}$. The 3 dB noise circles are close to $\Gamma^G_{\rm opt}$ or S^*_{11}. Excellent agreement is not expected because these are results for extrinsic FET's, while the theory is derived for intrinsic FET's. Many extrinsic FET's are only conditionally stable (K is less than 1) at the frequency where they are used for low-noise amplifiers, because of feedback from C_{gd}. Therefore, $\Gamma^G_{\rm opt}$ is undefined for maximum available gain and the simple 3 dB noise figure rule cannot be applied.

The difference between $R_{\rm opt}$ and r_{gs} increases as $F_{\rm min}$ decreases [(8)]. The noise figure of a FET matched for maximum gain remains close to 3 dB as noise figure decreases. This produces wider noise circles because the center of the 3 dB noise circle moves from $\Gamma^G_{\rm opt}$ as $F_{\rm min}$ decreases. One reason wider noise circles are sought is to obtain both high gain and good input match without increasing the noise figure significantly above $F_{\rm min}$. Apart from choosing the optimum FET gate width, the resistor temperature model shows that the only technique for making the noise circles of intrinsic FET's broader is to reduce $F_{\rm min}$. A lower $F_{\rm min}$ moves $\Gamma_{\rm opt}$ farther from $\Gamma^G_{\rm opt}$. The noise figure for Γ_G close to $\Gamma^G_{\rm opt}$ does not improve. If the $F_{\rm min}$ of the FET is increased, $\Gamma_{\rm opt}$ is closer to $\Gamma^G_{\rm opt}$, but the noise figure for Γ_G near $\Gamma^G_{\rm opt}$ is a little worse. The model shows that it is not possible to design an intrinsic FET (no feedback) with a noise figure less than 3 dB when matched for gain. For FET's with high noise figures (e.g., operating at a frequency closer to $f_{\rm max}$), there is little difference between matching for gain or minimum noise for a given bias. The other technique to bring $\Gamma_{\rm opt}$ and $\Gamma^G_{\rm opt}$ closer is to use reactive negative feedback (e.g., source inductance). This does not change $F_{\rm min}$ significantly, but it does reduce $G_{A\rm opt}$ substantially.

Experimentally, MODFET's designed for lower F_{min} with lower gate resistance and an optimum doping profile also had a lower R_n [19], [20]. The lower R_n was attributed to the high g_m of their MODFET design, and no direct correlation between R_n and $F_{\rm min}$ was noted. However, the correlation supports the suggestion made in this paper that a lower $F_{\rm min}$ results in a lower R_n and broader noise circles.

VII. Optimum Gate Width for Broad Noise Circles

The noise circles of a FET are broadest when $|\Gamma_{\rm opt}|$ is smallest. This occurs when the real part of $\Gamma_{\rm opt}$ is zero. An expression for the optimum gate width $W_{\rm opt}$ is found by solving for this condition.

$$W_{\rm opt} = \frac{R_{\rm opt}\cdot W}{50}(1+Q^2_{\Gamma_{\rm opt}})^{1/2} = \frac{1}{2\pi f\left(\frac{C_{\rm opt}}{W}\right)50}\left(\frac{1}{(2\pi fC_{\rm opt}R_{\rm opt})^2}+1\right)^{1/2}. \tag{17}$$

Substituting $R_{\rm opt}$ from (8) into the definition of $Q_{\Gamma\rm opt}$ gives

$$Q_{\Gamma_{\rm opt}} = \frac{1}{2\pi fC_{\rm opt}R_{\rm opt}} = \frac{T_{\rm min}}{2\pi fC_{\rm opt}r_{gs}(2T_g+T_{\rm min})}. \tag{18}$$

$Q_{\Gamma\rm opt}$ is independent of gate width if the FET parameters scale simply with gate width, as described earlier. $R_{\rm opt}$ is inversely proportional to frequency (see Fig. 3). Therefore, $Q_{\Gamma\rm opt}$ is a very weak function of frequency and $W_{\rm opt}$ is inversely proportional to frequency. Simple expressions are written for $R_{\rm opt}$ and $C_{\rm opt}$ for a FET of optimum gate width.

$$R_{\rm opt}(W=W_{\rm opt}) = 50\cdot(1+Q^2_{\Gamma_{\rm opt}})^{-1/2} \tag{19}$$

$$C_{\rm opt}(W=W_{\rm opt}) = \frac{1}{2\pi f50}\left(\frac{1}{Q^2_{\Gamma_{\rm opt}}}\right)^{1/2}. \tag{20}$$

$R_{\rm opt}(W=W_{\rm opt})$ is approximately independent of frequency, and $C_{\rm opt}(W=W_{\rm opt})$ is inversely proportional to

frequency. Substituting the approximate expression for R_{opt} [(8)] in (18) gives a good approximation for $Q_{\Gamma\text{opt}}$

$$Q_{\Gamma_{\text{opt}}} = \frac{1}{2\pi f_{\max} C_{\text{opt}} r_{gs}} \left(\frac{T_d}{4T_g}\right)^{1/2} = A_f \left(\frac{T_d}{4T_g}\right)^{1/2} \tag{21}$$

C_{opt} equals C_{gs} for the intrinsic FET model, and A_f is defined as $1/(2\pi f_{\max} C_{gs} r_{gs})$. When a FET is designed with a shorter gate length to increase $f_{\max}$ and reduce $F_{\min}$, the thickness of the active layer and the parasitics are usually reduced in proportion to $f_{\max}$ to achieve optimum performance [21]. If the FET is scaled correctly, then $Q_{\Gamma\text{opt}}$ does not change as $f_{\max}$ is increased. Optimum FET design principles [21] and experimental results show that: 1) C_{gs}/W should have a limited range, typically 0.8–1.2 pF/mm; 2) A_f is typically 2; and 3) $r_{gs} \cdot W$ is scaled inversely proportional to $f_{\max}$ (e.g., $f_{\max} \cdot r_{gs} \cdot W$ is typically 80 GHz $\cdot\Omega\cdot$ mm for a low-noise FET). T_g is ambient (300 K) and the effective T_d of extrinsic FETs is typically between 500 and 700 K for all frequencies (8–94 GHz), gate lengths (0.1–0.8 μm) and III–V material types [2]. Therefore, $Q_{\Gamma\text{opt}}$ is typically 1.2 independent of frequency and gate length (or $f_{\max}$). Note that the experimental $Q_{\Gamma\text{opt}}$ values given in Table I are close to this value.

$Q_{\Gamma\text{opt}}$ is a weak function of $T_{\min}$ or $f_{\max}$ [(18) and (21)] if T_g and T_d are constant and the FET is scaled correctly for gate length (C_{gs}/W is constant and r_{gs} is proportional to $1/f_{\max}$). Therefore, the $R_{\text{opt}}, X_{\text{opt}}$, and Γ_{opt} of a FET of optimum width are a weak function of frequency, $T_{\min}$ and $f_{\max}$. $R_{\text{opt}}(W_{\text{opt}}), X_{\text{opt}}(W_{\text{opt}})$, and $|\Gamma_{\text{opt}}(W_{\text{opt}})|$ are 32 Ω, 38 Ω, and 0.47, respectively for a typical $Q_{\Gamma\text{opt}}$ of 1.2. Equation (6) shows that when $T_{\min}$ (or $F_{\min}$) is reduced by reducing the gate length and correctly scaling the FET, then the noise circles become wider because $\Gamma_{\text{opt}}(W_{\text{opt}})$ changes negligibly. The ratio of the equivalent input noise temperature of a FET with a 50 Ω generator impedance, $T_e(50\,\Omega)$, to $T_{\min}$ is a weak function of frequency, $T_{\min}$, and $f_{\max}$ for low-noise FET's of optimum width because $\boldsymbol{n}$ and $|\Gamma_{\text{opt}}(W_{\text{opt}})|$ always have values close to 2 and 0.47, respectively (see (6) for Γ_G of 0). The $T_e(50\,\Omega)/T_{\min}$ ratio is typically 1.59 and $F(50\,\Omega)$ is typically $1.59 \cdot F_{\min} - 0.59$ for a FET of optimum width.

Substituting the $1/f$ approximation for R_{opt} [(8)], C_{gs} for C_{opt}, and the expressions for A_f into (18) gives a simple expression for W_{opt}

$$W_{\text{opt}} = \frac{1}{2\pi f \left(\frac{C_{gs}}{W}\right) 50} \left[\frac{4T_g}{A_f^2 T_d} + 1\right]^{1/2}. \tag{22}$$

For frequencies less than half $f_{\max}$, the $1/f$ approximation for R_{opt}/r_{gs} was 5% less than the full expression; therefore, this W_{opt} approximation is 3% less than the W_{opt} calculated from (18). W_{opt} is plotted as a function of frequency in Fig. 7 for typical values of C_{gs}/W (1.0 pF/mm), $A_f(2), T_d$ (500 K), and T_g (300 K). With these parameter values, the W_{opt} expression becomes approximately $3.9/f$(GHz) mm.

Equation (3) for gain circles is similar to (2) for noise circles. An expression can be written for the optimum gate

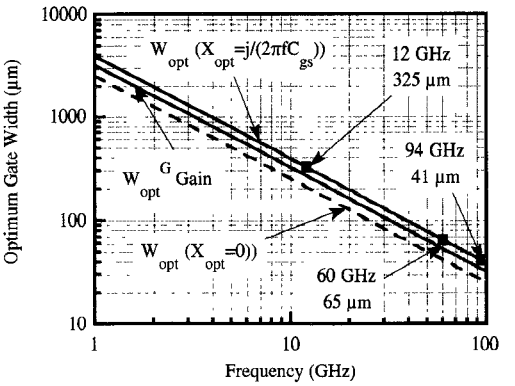

Fig. 7. Plots of optimum gate widths for broadest noise circles (W_{opt}) and broadest gain circles (W_{opt}^G) versus frequency for a FET with a C_{gs}/W of 1.0 pF/mm, an A_f of 2, a T_d of 500 K, and a T_g of 300 K. The broken line is W_{opt} for FET's with gate inductance such that X_{opt} is zero.

width for the broadest gain circles W_{opt}^G which is like the expression for W_{opt} [(7)]. The input Q of a typical FET is much greater than 1 at frequencies much less than $f_{\max}$ where $F_{\min}$ is low. Therefore, the W_{opt}^G is approximately the gate width that gives an input reactance of 50 Ω. For a FET with a typical input capacitance of 1.0 pF/min, W_{opt}^G is approximately $3.2/f$(GHz) mm. W_{opt}^G is plotted as a function of frequency in Fig. 7. The optimum width for broadest noise circles is approximately 20% larger than the optimum width for broadest gain circles.

$|\Gamma_{\text{opt}}|$ is smaller if X_{opt} (and $X_{\text{opt}} \cdot W$) is smaller. Therefore, a FET with a larger effective C_{opt}/W will have broader noise circles, if everything else is the same. The C_{gs}/W of a FET cannot be altered significantly without degrading FET gain. However, a lossless gate inductance in series with C_{gs} increases the effective C_{opt}. For example, bond wire to a FET chip has little loss at 12 GHz. If the inductance is chosen to resonate with C_{gs}, then X_{opt} is zero and the new optimum FET width gives an R_{opt} of 50 Ω. For this case, a FET has the broadest noise circles possible for a given $F_{\min}$. The expression for W_{opt} with X_{opt} equal to zero is

$$W_{\text{opt}}(X_{\text{opt}} = 0) = \frac{R_{\text{opt}} \cdot W}{50} \approx \frac{r_{gs} \cdot W}{50} \frac{f_{\max}}{f} \left(\frac{4T_g}{T_d}\right)^{1/2} = \frac{1}{2\pi f \left(\frac{C_{gs}}{W}\right) A_f 50} \left(\frac{4T_g}{T_d}\right)^{1/2}. \tag{23}$$

W_{opt} is plotted versus frequency in Fig. 7 for a FET with X_{opt} equal to zero. W_{opt} is smaller for X_{opt} equal to zero at a given frequency. For a typical FET, $W_{\text{opt}}\,(X_{\text{opt}} = 0)$ is 64% of W_{opt}. With the parameter values used to calculate W_{opt} for a typical FET, the $W_{\text{opt}}\,(X_{\text{opt}} = 0)$ expression becomes approximately $2.5/f$(GHz) mm. W_{opt}, for X_{opt} equal to zero, is again independent of gate length if the FET is scaled correctly such that C_{gs}/W and A_f are constant (and assuming T_d is constant).

Many simplifications were made in the expression for W_{opt}. More rigorous analysis and design are necessary to achieve

W_{opt} for real extrinsic FET processes. For example, the C_{gs}/W of 0.1 μm InP-based MODFET's is typically lower (0.7 pF/mm [22]) than 0.25 μm conventional GaAs-based MODFET's (1.0–1.15 pF/mm [12], [13], [17]).

The values of W_{opt} suggested in Fig. 7 are reasonable for the experimental results given in this paper. It is interesting to compare the optimum width for broadest noise circles suggested in Fig. 7 to the widths of low-noise FETs used in practice where there has been no discussion of choosing an optimum width for the broadest noise circles. At 94 GHz, widths of 30 and 40 μm are common [24]–[30]; these values are between the W_{opt} and W_{opt} ($X_{\text{opt}} = 0$) values suggested in Fig. 7, (41 and 26 μm, respectively). The most common width for 12 GHz DBS MODFET's is 200 μm [11]–[13], [17], [19], [20], [23]. The model presented in this paper suggests that the optimum width for broadest noise circles for a FET used in an MMIC circuit at 12 GHz is much larger at 325 μm. However, most DBS MODFET's are intended for hybrid IC circuits where low loss bond wire inductors are used. The model suggests a W_{opt} ($X_{\text{opt}} = 0$) of 208 μm; virtually the same as a typical DBS MODFET's. The agreement between model and practice is probably not a coincidence. It is very likely that experience had shown it was easier to design hybrid DBS amplifiers with MODFET's of 200 μm width. The optimum widths for broadest noise circles suggested by the model are close to those widths used in practice for both 0.1 μm MODFET's at 94 GHz and 0.25 μm MODFET's at 12 GHz.

VIII. Conclusions

The keys to broader noise circles are a FET with a lower $F_{\min}$ and a smaller $|\Gamma_{\text{opt}}|$. The lower $F_{\min}$ of MODFET's compared to GaAs MESFET's of the same gate length can explain the observation that MODFET's have wider noise circles [31]. There is an optimum gate width where $|\Gamma_{\text{opt}}|$ is the smallest and the angle of Γ_{opt} is 90°. The noise circles are broadest at this optimum width if the FET is scaled so that the input resistance is inversely proportional to width and $F_{\min}$ is independent of width. The FET width should be scaled by adding gate fingers in parallel.

The noise circle equation was written using a normalized parameter $\boldsymbol{n}, 4NT_o/T_{\min}$. $\boldsymbol{n}$ is a weak function of frequency and gate width. It has a limited range of values and it is close to 2 for low-noise FET's. Consequently, noise circles are easily estimated if Γ_{opt} and $F_{\min}$ are known.

For intrinsic low-noise FET's (e.g., $F_{\min}$ less than 1.5 dB) $T_{\min}$ is proportional to frequency; R_{opt} and the associated gain, $G_{A\text{opt}}$, are inversely proportional to frequency. The circuit-model parameters scale simply with gate width, so $F_{\min}$ and $G_{A\text{opt}}$ are independent of gate width, and R_{opt} is inversely proportional to width. The width independence was experimentally verified. A plot of Γ_{opt} as a function of gate width is a constant Q contour. The Q is almost independent of frequency. The optimum gate width for broadest noise circles is inversely proportional to frequency. Q is a weak function of gate length for low-noise FET's if the FET's are scaled optimally (e.g., C_{gs}/W is constant, r_{gs} is proportional to $1/f_{\max}$, the effective temperature of the output resistor of the extrinsic FET, T_d, is constant, etc.). Then the Γ_{opt}'s of FET's of optimum width W_{opt} are independent of frequency and gate length (or $f_{\max}$). For a typical low-noise FET of optimum width, Γ_{opt} has a magnitude of 0.47 and an angle 90°.

The noise figure of an intrinsic FET matched for gain is greater than 3 dB and close to 3 dB for low-noise FET's. This is because the input and generator resistances are equal for a matched input and their temperatures are approximately 290 K. Both resistors produce equal noise power. The input noise is much larger than the output noise for a low-noise FET matched for gain because it is amplified by $G_{A\max}$. With this 3 dB rule, one can understand why noise circles are broader when the difference between the reflection coefficient for maximum gain and minimum noise figure is largest. The difference is larger when a FET has a lower $F_{\min}$ and a higher $f_{\max}$.

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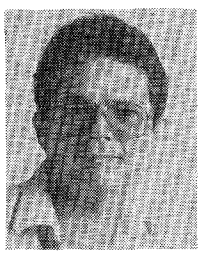

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